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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/718,503

11/19/2003

Mark L. DiOrio

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27906

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08/11/2004

PATENT LAW OFFICES OF DAVID MILLERS
6560 ASHFIELD COURT
SAN JOSE, CA 95120

EXAMINER

NGUYEN, JIMMY

ART UNIT

PAPER NUMBER

2829

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/718,503	Applicant(s) DIORIO, MARK L.	
	Examiner Jimmy Nguyen	Art Unit 2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 March 2004.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-21 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>0704</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 11/19/03 is being considered by the examiner.

Oath/Declaration

It is missing the second inventor's signature. Correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Farnworth et al (US 6426639).

As to claim 1, Farnworth et al disclose (fig 7) a probe process comprising:

brings the probe tips (60) into contact with external terminals (70a) on the package (40a) , therefore Farnworth et al teach the step of bringing the probe tips,

uses the probe tips (60) to deform (column 11 line 67 and column 12 line 1

– 15) the terminals (70a) to improve planarity of the external terminals (70a);

therefore Farnworth et al teach the step of using the probe tips to deform the terminals to improve planarity (when the probe tips(60) come to contact with the terminals (70a) as shown in figure 7 the probe tips (60) will deform the shape of terminal (70a) and create a planarity contact surface on terminal because the probe (60) has the flat contact surface (65)).

electrically testing (it is inherent that the test apparatus 10 must connect with the tester to transmit and perform the test) the device (40a) through electrical connections of the probe tip (60) to the external terminals, therefore Farnworth et al teach the step of testing.

It is inherent that the probe card or the testing apparatus must connect to the tester or the testing equipment to perform the testing. In this case, Farnworth et al only disclose the probe card or the testing apparatus in figure 7 but the tester is not shown, therefore, the tester to perform the testing procedure is inherently within the scope of Farnworth et al's invention.

As to claim 11, Farnworth et al disclose (fig 7) the external terminals form a BGA (40A)

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 12 is rejected under 35 U.S.C. 102(b) as being anticipated by Okubo et al (US 5055778).

As to claim 12, Okubo et al disclose probe apparatus comprising:

connects a printed circuit board (12) to test equipment (not shown but inherently must have the tester in order to perform the test) , wherein the printed circuit board (12) includes a set of contact pads (331 connect to probes 30) having a pattern that matches elevated terminals (661) on a device (60) to be tested; therefore Okubo et al teach the step of connecting.

brings the printed circuit board (12) and the device (60) into contact so that the elevated terminals (611) on the device (60) make electrical connections with the contact pads (331 connect to probes 30) on the printed circuit board (12); therefore Okubo et al teach the step of bringing, and

uses the test equipment (not shown but inherently must have the tester in order to perform the test) to test the device (60) via the electrical connections of the printed circuit board (12) to the device (60), therefore Okubo et al teach the step of using.

It is inherent that the probe card or the testing apparatus must connect to the tester or the testing equipment to perform the testing. In this case, Okubo et al only disclose the probe card or the testing apparatus in figure 1 but the tester is not shown, therefore, the tester is inherently within the scope of Okubo et al's invention.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1 - 4, 6, 10, 16, 18, 21, are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al (US 6426639) in view of Sano (US 5604446).

As to claims 1, 16, 18, Farnworth et al disclose (fig 7) a probe apparatus comprising:

brings the probe tips (60) and terminals (70a) on a device (40a) into contact, therefore Farnworth et al teach the step of bringing the probe tips,

uses the probe tips (60) to deform (column 11 line 67 and column 12 line 1 – 15) the terminals (70a) to improve planarity of the terminals (70a); therefore Farnworth et al teach the step of using the probe tips to deform the terminals to improve planarity (when the probe tips(60) come to contact with the terminals

(70a) as shown in figure 7 the probe tips (60) will deform the shape of terminal (70a) and create a planarity contact surface on terminal because the probe (60) has the flat contact surface (65)).

However, Farnworth et al are silent on electrically testing the device through electrical connections of the probe tip to the terminals.

On the other hand, Sano teaches the apparatus of electrically testing (by tester 69, fig 1) the device (W) through electrical connections of the probe tip (14) to the terminals (on the W), therefore Sano teaches the step of testing. Further, Sano is also disclose the mechanism (which is the probe itself has the capability to press the probe tip down to contact with the solder ball on dut) capable of pressing external terminals of a package against the probe tips with sufficient force.

It would have been obvious to one having an ordinary skill in the art at the time of invention was made to use the tester of Sano within the testing apparatus of Farnworth et al for the purpose of testing the characteristic of lcs.

As to claims 2, 3, Sano discloses (fig 3) the bringing the probe tips (14) into contact with the external terminals (on the W) comprises plugging the package into a socket (work table 13) and apply the pressure to deform the external terminals

As to claim 4, Farnworth et al disclose (fig 7) each probe tip (60) has a flat contact area (65) and flattens (when the probe tips 60 come to contact with the solder ball 70a, it will create a flat surface on the solder ball under the contact pressure) a corresponding one of the terminals (70a), while simultaneously providing an electrical connection (by coming to contact of the probe 60) to the terminals (70a).

As to claim 6, Farnworth et al disclose (fig 7) the probe tips (60) are affixed to the substrate (30).

As to claims 10, 21, Farnworth et al disclose (fig 10 A) the probe tips (23, 30a) have sizes that depend on distances from a center point (30a) so that the probe tips (23, 30a) can be aligned to contact the terminals (71) over a range of temperatures (the width of center point 30a must align with the terminal 71 otherwise it not come to contact. Further, the substrate and the die have the same coefficient of thermal expansion (column 13 line 59 – 62), therefore it provides the same range of temperature).

7. Claims 5, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth (US 6426639).

As to claims 5, 17, Farnworth et al illustrated (fig 9) the flat contact area (23) has a width that is at least one half of a width of one of the terminals (71a) (the

flat contact area 23 has the center portion 24 which has the length run from one side of the solder ball to the end of substrate 10 are approximately twice the diameter of the solder ball.)

It would have been obvious to one having an ordinary skill in art to recognize the flat contact area 23 has the length that at least one half of the terminals to ensure the good contact between the test apparatus and the device.

8. Claims 7 – 9, 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al (US 6426639) in view of Sano (US 5604446) and further in view of Okubo et al (US 5055778).

As to claim 7, Farnworth et al and Sano et al have disclosed the probing apparatus, which anticipated the probing process as explained in the base claims 1 and 4. However, Farworth et al and Sano et al are silent on the above combination with the substrate as a printed circuit board.

On the other hand, Okubo et al teach the substrate (10, 12) as a printed circuit board (12).

It would have been obvious to one having an ordinary skill in the art at the time of the invention was made to replace the substrate in testing apparatus of Farnworth et al and Sano for the printed circuit board of Okubo et al for the benefit of reducing noise during testing and transmitting signal.

As to claims 8, 9, 19, 20, Okubo et al disclose the probe tips (30) comprise bonding pads (331) and bumps (331) disposed on a surface of the printed circuit board (12).

9. Claims 13 - 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okubo et al (US 5055778) in view of Sano (US 5604446).

As to claim 12, Okubo et al disclose probe apparatus comprising:

connects a printed circuit board (12) to test equipment (not shown) , wherein the printed circuit board (12) includes a set of contact pads (331 connect to probes 30) having a pattern that matches elevated terminals (661) on a package containing a device (60) ; therefore Okubo et al teach the step of connecting.

brings the printed circuit board (12) and the package (60) into contact so that the elevated terminals (611) on the device (60) make electrical connections with the contact pads (331 connect to probes 30) on the printed circuit board (12); therefore Okubo et al teach the step of bringing.

However, Okubo et al are silent on the step of using the test equipment to test the device via the electrical connections of the printed circuit board to the package .

On the other hand, Sano discloses (fig 1) the apparatus of use test equipment (69) to test the device (W) via the electrical connections of the printed board (42, fig 3) therefore Sano teaches the step of using.

It would have been obvious to one having an ordinary skill in the art at the time of invention was made to use the tester of Sano within the testing apparatus of Farnworth et al for the purpose of testing the characteristic of lcs.


As to claim 13, Okubo et al disclose (fig 1) the contact pads (331 connect to probes 30) on the printed circuit board (12) directly contact the elevated terminals (611) of the package (60) to make the electrical connection.

As to claim 14, Okubo et al disclose (fig 1) the contact pads (331 connect to probes 30) on the printed circuit board (12) comprise bumps (331) that directly contact the elevated terminals (661) to make the electrical connections.

As to claim 15, Okubo et al disclose (fig 1) the elevated terminals (611) comprise solder balls.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen at (571) 272- 1965. Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to Kamine Cuneo (SPE 2829) whose telephone number is (571) 272- 1957.


DAVID ZARNEKE
PRIMARY EXAMINER